

## APPLICATION

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resulting in the formation of a silicide layer on the top of the polysilicon electrode. Silicide is hard to etch, and it acts as a barrier to complete removal of polysilicon.

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#### DESCRIPTION OF THE DRAWINGS

Figs. 1 - 16 are cross-sectional views of a semiconductor device structure at various stages of fabrication.

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Figs. 17 - 19 are cross-sectional views of the semiconductor device structure at alternative stages of fabrication.

#### DESCRIPTION

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Referring to Fig. 1, a semiconductor substrate 10 has a gate oxide layer 12 and a polysilicon layer 14 deposited thereon. Gate oxide layer 12 has a thickness  $T_1$  suitable for use in transistors, e.g., 10-25 Ångstroms (Å), preferably 15 Å. Polysilicon layer 14 has a thickness  $T_2$  suitable for a gate electrode in a transistor of, for example, 2600 Å.

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Referring to Fig. 2, a photoresist is dispensed upon polysilicon layer 14 and patterned to form a photoresist masking feature 16. Photoresist masking feature 16 has a

width  $W_1$  suitable for a transistor channel length, e.g., of 0.03 micrometers ( $\mu\text{m}$ ).

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Etch DPS II Centura<sup>TM</sup> 300 system, manufactured by Applied Materials, Inc., Santa Clara, California. Portions of polysilicon layer 14 and gate oxide layer 12 not in a shadow of photoresist masking feature 16, i.e. not underneath feature 16, are removed during etching. The etching thereby forms a polysilicon gate electrode 18.

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Referring to Fig. 4, photoresist masking feature 16 is stripped off, leaving polysilicon gate electrode 18 and gate oxide 12 on silicon substrate 10.

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Referring to Fig. 5, a first ion implantation is made into silicon substrate 10 to form a lightly doped source region 20 and a lightly doped drain region 22. For a p-channel device, a p-type dopant, such as boron, may be implanted into lightly doped source 20 and lightly doped drain 22 regions.

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Referring to Fig. 6, a first sidewall spacer 24 and a second sidewall spacer 26 are formed proximate a first side 28 and a second side 30 of polysilicon gate electrode 18, respectively. First and second sidewall spacers 24, 26 are

formed by the deposition of, e.g., a silicon dioxide sidewall spacer layer by, for example, low pressure chemical vapor deposition (LPCVD), followed by the deposition of, e.g., a silicon nitride sidewall spacer layer, also by LPCVD. The LPCVD of both the silicon dioxide and silicon nitride sidewall spacer layers is done in a furnace, such as VERTRON®V(S) furnace, manufactured by Kokusai Semiconductor Equipment Corporation, Billerica, Massachusetts. Deposition of sidewall spacer layers is followed by etchback in a dry etching system to define first and second sidewall spacers 24, 26. The dry etching system is, for example, the Unity® with a dipole ring magnet (DRM) plasma source, manufactured by Tokyo Electron, with headquarters in Austin, Texas.

Referring to Fig. 7, a second ion implantation is made into silicon substrate 10 to form a source 32 and a drain 34 region. For a p-channel device, a p-type dopant, such as boron, is implanted into source 32 and drain 34 regions.

Referring to Figs. 8 and 9, a metal such as cobalt is deposited over substrate 10 and polysilicon gate electrode 18 to form a cobalt layer 40. Cobalt layer 40 is deposited by a deposition method such as sputtering in a system such as the Endura®, manufactured by Applied Materials, Inc. Cobalt layer 40 has a thickness  $T_3$  of, e.g., 200 Å.

Substrate 10 and cobalt layer 40 are heated in, for example, a rapid thermal processing system, such as the RTP XE Centura® system, manufactured by Applied Materials, Inc. At an elevated temperature, such as 700°C, for a short period, such as 45 seconds, cobalt layer 40 reacts with silicon to form a first cobalt silicide region 42 over source 32, a second cobalt silicide region 44 over drain 34, and a third cobalt silicide region 46 over polysilicon gate electrode 18. First, second, and third cobalt silicide regions 42, 44, 46 have a thickness  $T_3'$  of 500 Å. Unreacted cobalt, i.e. cobalt which does not react with silicon to form cobalt silicide, over dielectric layers, such as cobalt over first and second sidewall spacers 24, 26, is removed with a wet etch, such as a mixture of sulfuric acid, hydrogen peroxide, and DI water.

Referring to Fig. 10, silicon nitride is deposited over substrate 10 to form a silicon nitride etch stop layer (NESL) 50. NESL 50 is formed by, e.g., plasma enhanced chemical vapor deposition (PECVD) in a system such as the Producer®, manufactured by Applied Materials, Inc. NESL 50 has a thickness  $T_4$  of, e.g., 500 Å, sufficient to serve as an etch stop during a subsequent contact etch. Subsequently, an interlevel dielectric, such as silicon dioxide, is deposited over NESL 50 to form interlevel oxide

layer 52. Interlevel oxide layer 52 is formed by a deposition process, for example by PECVD in a system such as the Producer®, manufactured by Applied Materials, Inc. Interlevel oxide layer 52 has a thickness  $T_5$  of, for example, approximately twice the height of the polysilicon thickness, e.g. 5000 Å. This thickness  $T_5$  is sufficient to provide complete coverage of polysilicon gate electrode 18, without being too thick and thereby wasting material.

Nitride layer 50 and interlevel oxide layer 52 follow the topography of the underlying structure, including gate electrode 18 and substrate 10. These layers 50, 52 have, therefore, a high region 54 above gate electrode 18 and a first low region 56 and a second low region 58 above source 32 and drain 34, respectively.

Referring to Fig. 11, silicon substrate 10 is polished in a chemical mechanical polishing (CMP) system, such as the Reflexion™ system, manufactured by Applied Materials, Inc. The CMP system removes high region 54 of interlevel oxide layer 52 and nitride layer 50, leaving behind first and second low regions 56, 58 of interlevel oxide 52 and nitride 50 layers over source 32 and drain 34, respectively. Interlevel oxide layer 52 and nitride layer 50 left behind in low regions 56, 58 serve as a mask for protecting underlying features. The removal of high region

54 of interlevel oxide 52 and nitride 50 layers results in the exposure of cobalt silicide region 46 over gate electrode 18.

Referring also to Fig. 12, chemical mechanical polishing is continued to remove cobalt silicide region 46 from a top surface 60 of polysilicon gate electrode 18. The chemical mechanical polishing is performed with a slurry providing a relatively low polishing rate for polysilicon 18, a relatively high rate for interlevel silicon dioxide 52, and a sufficiently high polishing rate for silicon nitride 50 and cobalt silicide 46 to achieve the structure illustrated in Fig. 12. The ratio of polishing rates of polysilicon: silicon dioxide: silicon nitride: cobalt silicide is 1:10:7:7 in this embodiment. Cobalt silicide region 46 is removed from gate electrode 18, while interlevel oxide layer 52 and nitride layer 50 in low regions 56, 58 over source 32 and drain 34 are left intact. An example of a suitable slurry that provides the necessary polishing rate selectivities is Semi-Sperse® 10 manufactured by Cabot Microelectronics, based in Aurora, Illinois. During polishing, this slurry is diluted to 25% slurry/75% DI water by the addition of DI water to the slurry in the slurry distribution system.



Referring also to Fig. 13, after the removal of cobalt silicide 46 over gate electrode 18, gate electrode 18 is removed by a wet etch, e.g., by ammonium hydroxide, or by a dry etch with, e.g. hydrogen bromide/chlorine/oxygen, leaving a cavity 70 and exposing a top surface 72 of gate oxide layer 12. The wet etch or dry etch is highly selective to gate oxide. Gate oxide layer 12 may be damaged by deposition and removal of polysilicon.

Referring also to Fig. 14, gate oxide layer 12 is removed by a wet etch, such as a solution of hydrofluoric acid, thereby exposing a surface 74 of substrate 10.

Referring to Fig. 15, a replacement gate oxide layer 76 is grown on surface 74 of substrate 10 to replace damaged gate oxide layer 12.

Referring to Fig. 16, a metal is deposited into cavity 70 to form a metal gate electrode 80. The metal is selected to have an appropriate work-function for the voltage level at which a transistor, including source 32, drain 34, and gate electrode 80, turns on and off. The metal forming metal gate electrode 80 is, for example, aluminum for an n-channel transistor.

Referring to Fig. 17, in a second embodiment, semiconductor substrate 10 is processed as described above with reference to Fig. 1 through Fig. 10. After the

deposition of NESL layer 50 and interlevel oxide layer 52, a material is deposited to form top layer 90 on top of interlevel oxide layer 52 and NESL 50. Top layer 90 has a chemical structure different from that of interlevel oxide layer 52. An example of a material suitable for deposition as top layer 90 is a material with a substantially different chemical-mechanical polishing rate from that of the underlying interlevel oxide layer 52, e.g., titanium nitride. Top layer 90 has a thickness  $T_5$  of, e.g., 3000 Å.

Referring to Fig. 18, top layer 90 is polished in a CMP system, such as the Reflexion®, manufactured by Applied Materials, Inc. Top layer 90 is polished faster than interlevel oxide layer 52 when a first slurry is used, i.e. the polishing rate of top layer 90, comprising titanium nitride, is greater than the polishing rate of the dielectric layer including interlevel oxide layer 52. An example of a suitable first slurry is Semi-Sperse® W2000, manufactured by Cabot Microelectronics. As a result, top layer 90 is removed from high region 54, exposing interlevel oxide 52 in high region 54. Top layer 90 remains as a mask in low regions 56, 58.

Referring to Fig. 19, a chemical mechanical polish is performed with a second slurry that causes top layer 90 to be polished more slowly than interlevel oxide layer 52 and

NESL 50, i.e. the polishing rate of titanium nitride with the second slurry is less than the polishing rate of the dielectric layer comprising interlevel oxide layer 52 and NESL 50. An example of the second slurry is Semi-Sperse® 10, manufactured by Cabot Microelectronics. Hence, the selectivity of the polishing of top layer 90 to interlevel oxide layer 52 is controlled. The CMP with the second slurry results in the exposure of cobalt silicide region 46.

Cobalt silicide region 46 is then removed as described above with reference to Fig. 12, and substrate 10 is processed according to the method described with reference to Figs. 13-16.

The invention is not limited to the specific embodiments described above. For example, an embodiment of the method can include the formation of an n-channel device, in which an n-type dopant, such as phosphorus, is implanted into the source and drain regions. The nitride etch stop layer can be omitted. The silicon dioxide layer can be doped. The polysilicon gate electrode can be etched out to form a cavity by a dry etch. The silicide layer can include a metal other than cobalt, such as titanium. The silicide layer can be formed by various methods, including by cosputtering a metal and silicon.

After removal of the polysilicon gate electrode and gate oxide, the gate oxide can be removed and replaced with a material with a high dielectric constant. After removal of the polysilicon gate electrode, removal of the gate oxide can be omitted, especially if, e.g., it is not damaged during the removal of the polysilicon, and a metal gate electrode can be formed on the original gate oxide. A barrier layer can be formed between the gate oxide and the metal gate electrode, such as a titanium nitride layer.

10 The metal gate electrode can include metals or metal alloys other than aluminum, such as titanium, aluminum or ruthenium.

Other embodiments not described herein are also within the scope of the following claims.

15 What is claimed is: